REMARKS/ARGUMENTS

Claims 1-4 and 8-19 remain in the application. Of these, claims 1-4, 8, 9, 17 and 19 stand allowed; claims 10-15 and 18 stand rejected; and claim 16 stands objected to as being dependent upon a rejected base claim, but is otherwise allowable.

1. Rejection of Claims 10-15 and 18 under 35 USC 102(e)

Claims 10-15 and 18 stand rejected under 35 USC 102(e) as being anticipated by Krech, Jr. et al (U.S. Pat. No. 6,779,140; hereinafter "Krech").

In rejecting claim 10, the Examiner asserts:

> . . .Krech teach detecting a remote instruction received from a remote controller (figure 2, item 5 through bus controller 88, ring bus, microcontroller to detect remote instruction 22); upon detecting the remote test instruction, switching from a control mode (local control include control mode that executes test program to be applied to the device (figure 1, blocks 4a, 6a) to control testing of a device, to a slave mode (slave site controller in slave mode condition) to pass through the remote test instruction to a tester (title; figures 1, test system controller through system bus at blocks 2, 3 and 5a).
>
> 8/22/2005 Final Office Action, p. 2, sec. 4.

Applicant respectfully disagrees. To begin, Krech does not teach that any of the "ALU instructions 22" are remote test instructions received from a remote controller, as is recited in Applicant's claim 10. Rather, Krech teaches that:

> . . .The Ring Bus 85 is the mechanism by which the Test Site Controller communicates with the APG portion of the DUT tester 6. The Ring Bus 85 is coupled to a Micro-Controller Sequencer 19, which may be likened to a special purpose microprocessor. Using an address created by a Next Address Calculator 102, it fetches instructions from a program stored in a program memory, which may be either internal to the Micro-Controller Sequencer 19 (PGM SRAM 20) or external thereto (EXT. DRAM 21). Although these two memories appear to be addressed by what is essentially a logically common address 63 that serves as a program counter (or, instruction fetch address), and

> either can be a source of programming to be executed, note that: (1) Only one of the memories performs instruction fetch memory cycles during any period of time; and (2) In fact they are addressed by electrically different signals. The SRAM is fast and allows genuine random access, but consumes valuable space within the Micro-Sequence Controller 19 (which is part of the large APG IC), so its size is limited. The external DRAM can be provided in adjustable amounts of considerable quantity, but is fast only when accessed in sequential chunks involving linear execution and no branching. Programming in the SRAM 20 is most often that which is intensely algorithmic, while the EXT. DRAM 21 is best suited for material not readily generated by algorithmic processes, such as initialization routines and random or irregular data.
>
> Krech, col. 11, line 64 - col. 12, line 18.

> The instruction word fetched and executed by the Micro-Controller Sequencer 19 is fairly wide: two hundred and eight bits. It consists of thirteen sixteen-bit fields. These fields often represent fetched instruction information for mechanisms that are outside the Micro-Controller Sequencer proper. Such fields are dedicated to their associated mechanisms. ***One set of ALU INSTRUCTIONS 22 are applied to a collection of eight sixteen-bit ALU's 24, while others are disbursed to various other mechanisms distributed throughout the DUT Tester.*** This latter situation is represented by the lines and legend "VARIOUS CONTROL VALUES & INSTRUCTIONS" 42.
>
> Krech, col. 12, lines 27-38. Emphasis added.

The above-emphasized sentence is Krech's only discussion of the "ALU instructions 22"; and Applicant can find no mention that 1) any of the instructions 22 is a "remote test instruction received from a remote controller", or 2) any "remote test instruction received from a remote controller" is "passed through" the DUT tester 6. Rather, it appears that A) the instructions 22 are generated or fetched locally by the "micro-controller sequencer 19" of the "DUT tester 6", and B) none of the instructions that are written into the external DRAM 21 via the ring bus 85 are "detected" by the micro-controller sequencer 19, and are instead fetched in accord with a local program executed by the micro-controller sequencer 19.

Furthermore, Applicant cannot find any mention by Krech that, upon detecting a remote test instruction, a local controller of a test system switches from a "control mode" to a "slave mode". Although Krech frequently discusses the operation of a test-site controller 6 in a "slave mode", Krech is talking about master-slave

relationships between different test-site controllers 6, and these master-slave relationships do not appear to be for passing "remote test instructions" to a tester (i.e., in lieu of a local controller of a test system initiating one or more test instructions to be applied to a device). *See*, e.g., Krech, col. 10, lines 4-7.

In light of the above arguments, Applicant believes the Examiner has failed to make a prima facie case for rejecting claim 10; and claim 10 should be allowed over Krech's teachings.

Applicant's claims 11-15 and 18 are believed to be allowable at least for the reason that they depend from applicant's claim 10.

2. Conclusion

Given the above Remarks and Arguments, Applicant respectfully requests the issuance of a Notice of Allowance.

Respectfully submitted,
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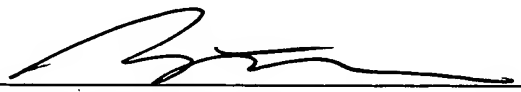
By: 

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